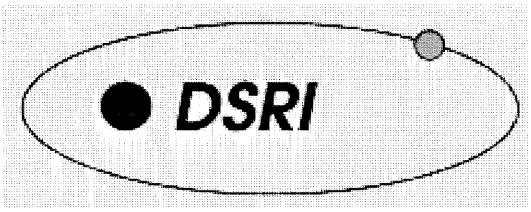

DANISH SPACE RESEARCH INSTITUTE

JEM-X FM1 Electrical Integration Test Report
(IN-TR-JEM-0030)

Date: 20 August 2001

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CONTENTS

1. SCOPE OF THE DOCUMENT

This document has been written in order to summarize all the test activities concerning the electrical verification of the JEM-X FM1 Instrument.

The test has been performed in DSRI (Copenhagen) using manual oscilloscope, digital voltmeter, current probe and BOB for the measurements.
Moreover, to perform the activities, the Satellite Interface Simulator (SIS) has been used.

Thus, detailed requirements and methodologies for the test execution together with the test instruments configuration will be provided within this document.

2. TEST OBJECTIVE

Purpose of the JEM-X FM1 electrical integration was to perform a test in order to check all the cable connections and the interfaces between the DFEE and the external world (DPE, SIS RTU and SIS PDU):

- to verify the equipment grounding;
- to verify all the equipment electrical interfaces characteristics w.r.t. all the applicable requirements;
- to verify the equipment compatibility w.r.t harness;
- to perform the harness connection.

3. REFERENCE DOCUMENTS

This section contains a list of documents filled with electrical interfaces necessary to organize and to detail the operative execution of the test activities.

- JEM-X EID-B Issue 5.2 (March 2000) JEMX/EID-B_5.2
- JEM-X User Manual 4.2 JEMX/UM_4.2

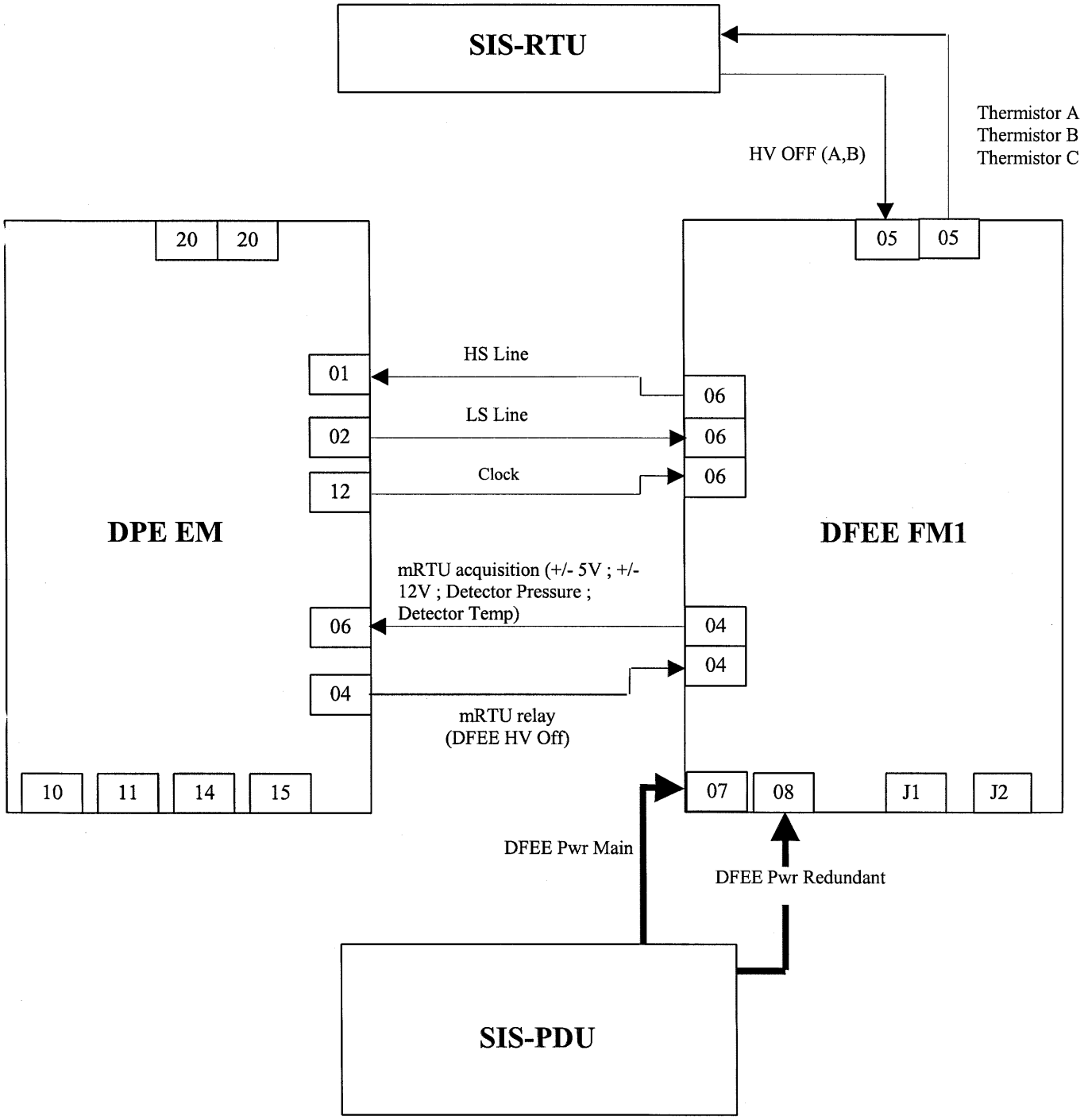
4. ANOMALIES and NCR

No anomalies have been discovered during the test activities and no NCR have been issued.

It has to be poited out that all the measures concerning the SIS-RTU / DFEE interfaces (connected and unconnected) has not been verified due to the lack of the connector cable between SIS-RTU and DFEE J05.

5. TEST SETUP

Here below is reported the set-up that will be carried out during the activities.



The tests has been performed first, unloaded and then loaded by means of a manual oscilloscope, digital voltmeter, current probe, BOBs (to put between the DFEE FM1 and the DPE EM to verify the signals interface) and long jumpers to detect the power consumption.

6. HARDWARE CONFIGURATION

In order to carry out the activity detailed in this procedure, the following hardware configuration was available:

- SIS PDU simulator;
- SIS RTU simulator;
- On-Board Data Handling (OBDH FEE);
- DPE (EM);
- DFEE (FM1);
- Detector & DAE (FM1).

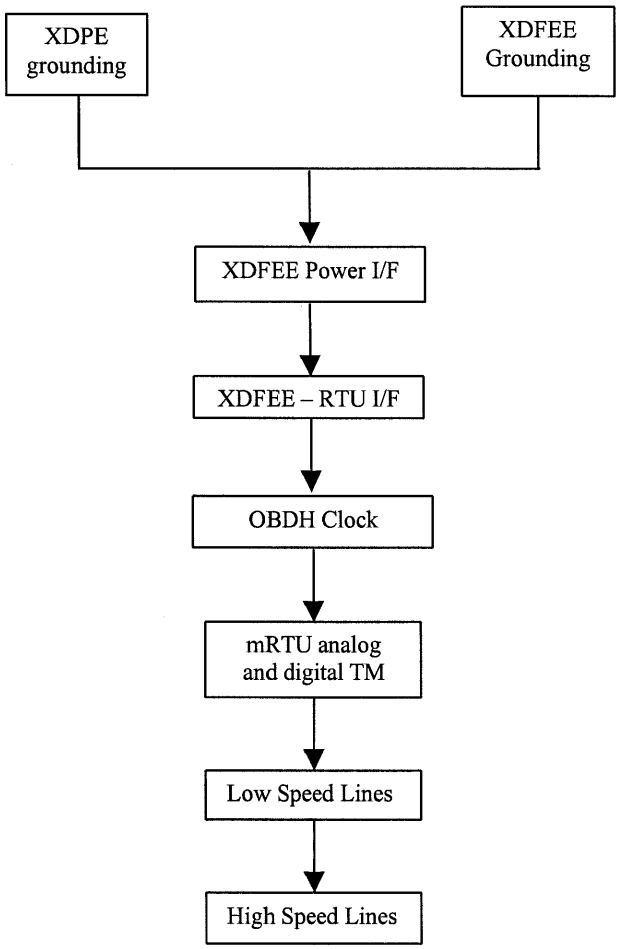
7. MEASUREMENTS TOOLS

In order to carry out the activity detailed in this procedure, the following tools will be used:

- Digital Multimeter;
- Oscilloscope;
- BOB:
  - N x 26 pins BOB;
  - N x 50 pins BOB;
  - N x 116 pins BOB;

8. TEST DESCRIPTION

In the following table the flow of all the foreseen tests is represented. For each test the verified connectors and interfaces are listed.



DFEE Grounding: With this test the grounding of the DFEE FM1 has been verified on the DFEE FM1 side. The involved connectors have different interfaces like LCL, SHP and ANY.

DFEE Power Interface: With this test the inrush current and steady state current of the signals from the SIS-PDU to the DFEE FM1 has been verified. The involved connectors have different interfaces like LCL.

DFEE RTU Interface: With this test the SIS-RTU signals to the DFEE FM1 has been verified. The involved connectors had different interfaces like SHP and ANY (just loaded test have been performed).

OBDH Clock: With this test the Litton code at the DPE connectors and the clock provided by the DPE EM have been verified.

mRTU analog and digital Interface: With this test the analog TM signals levels used to monitor the DFEE FM1 LVPS have been checked. The involved connectors had different interfaces like ANY, AND, BDI and SHP.

Low Speed Line Verification: With this test the Low Speed Lines between the DFEE FM1 and the DPE EM have been verified.

High Speed Line Verification: With this test the High Speed Lines between the DFEE and the DPE have been verified.

9. TEST PERFORMED

A list of all the tests executed during the electrical integration is following shown:
The Step-by-Step procedure is split in the following test:

- DFEE FM1 Pin Grounding Continuity Check
- DFEE FM1 Power Interface Verification
  - SIS-PDU / DFEE FM1 Interface Connected Check
- OBDH Clock Verification
- mRTU Analog and Digital Interface Verification
  - mRTU Analog and Digital I/F Verification Unconnected Check
  - mRTU Analog and Digital I/F Verification Connected Check
- Low Speed Serial Line Verification
- High Speed Serial Line Verification

10. AS-RUN PROCEDURE

The electrical I&T has been executed following the Test Procedure IN-TP-JEM-0012 document.
The as-run, which contains all the numerical results and electrical plots, is following attached.